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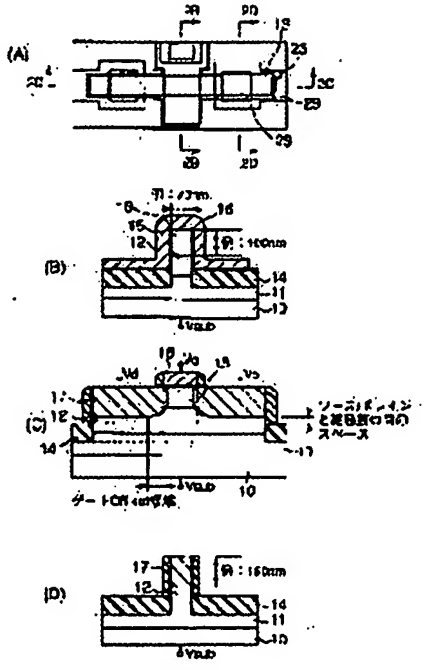
(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which has a structure capable of contriving an increase in the performance of the device and uses at least each one part of the side surfaces of projected semiconductor layers as a channel region.

SOLUTION: A semiconductor device is provided with projected semiconductor layers 13, source and drain regions 17 and 17 provided in the layers 13, and a gate electrode 16 which has a sidewall gate part provided in a state that the sidewall gate is insulated from these layers 13 on the side surfaces of the layers 13 and gives a field effect to a channel region between the regions 17 and 17 via at least the side surfaces of the layers 13. The distance between the regions 17 and 17 is changed on the side surfaces of the layers 13.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, The semiconductor device with which it provides and distance between said source fields and said drain fields is characterized by changing in two side faces in which it faces mutually [said convex semi-conductor layer].
[Claim 2] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and the side-attachment-wall insulator layer prepared on the side face of said gate electrode, and the side face of said convex semi-conductor layer.
[Claim 3] The convex semi-conductor layer prepared on the substrate, and the isolation insulator layer formed in the perimeter of the lower field of said convex semi-conductor layer, The source field and drain field which were prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to said channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, for the location of the top face of said isolation insulator layer being lower than the top face of said convex semi-conductor layer, and for the location of the deepest part of said source field and a drain field being the same as the location of the top face of said component demarcation membrane, or being lower than it.
[Claim 4] Said source field and a drain field are a semiconductor device according to claim 3 characterized by overlapping to said side-attachment-wall gate section.
[Claim 5] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate, Said 1st convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, and the 2nd convex semi-conductor layer with the same width of face, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. Said 1st side face and said 2nd side face are minded at least. The semiconductor device characterized by providing the gate electrode which gives the electric field effect to the 1st channel field between said 1st source fields and said 1st drain fields, and the 2nd channel field between said 2nd source fields and said 2nd drain fields.
[Claim 6] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate, The 2nd convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the

electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, The 1st wiring which connects mutually said 1st source field and said 2nd source field, The semiconductor device characterized by providing the 3rd wiring which connects the 2nd wiring which connects mutually said 1st drain field and said 2nd drain field, and said 1st gate electrode and said 2nd gate electrode of each other.

[Claim 7] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The source field and drain field which were prepared in said 1st convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer, And it has the gate contact section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the top face of said 2nd convex semi-conductor layer, respectively. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer.

[Claim 8] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The electric conduction object which possesses the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and constitutes said side-attachment-wall gate section is a semiconductor device characterized by differing from the electric conduction object which constitutes said top-face gate section.

[Claim 9] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and wiring electrically contacted by said gate electrode by the top-face upper part of said convex semi-conductor layer.

[Claim 10] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source fields and said 1st drain fields, and the 2nd channel field between said 2nd source fields and said 2nd drain fields through said 1st side face and said 2nd side face, The semiconductor device characterized by providing at least one 3rd convex semi-conductor layer of said 1st and 2nd source fields and said 1st and 2nd drain fields which connects either mutually at least.

[Claim 11] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field of the 1st conductivity type which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field of the 2nd conductivity type which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It is the semiconductor device characterized by providing and the depth of said 2nd source field and the 2nd drain field being deeper than the depth of said 1st source field and the 1st drain field.

[Claim 12] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which estrange mutually, are prepared in said 2nd convex semi-conductor layer, and have the same conductivity type as said 1st source field and said 1st drain field, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It is the semiconductor device characterized by providing and the depth of said 2nd source field and the 2nd drain field being deeper than the depth of said 1st source field and the 1st drain field.

[Claim 13] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, constituting said gate electrode including the 1st layer and the 2nd layer at least, and said gate electrode constituting the word line of semiconductor memory equipment.

[Claim 14] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, constituting said gate electrode including the 1st layer and the 2nd layer at least, and for said top face of the 1st layer being flat, and preparing said 2nd layer on said flat top face of the 1st layer.

[Claim 15] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing and said gate electrode being constituted including the 1st layer and the 2nd layer at least, and for said top face of the 1st layer having a step, preparing said 2nd layer on a top face with said step of the 1st layer, and said top face of the 2nd layer being flat.

[Claim 16] The convex semi-conductor layer which is prepared on a substrate and has the 1st side face, the 2nd side face which countered this 1st side face, the 3rd side face in which it is located between the 1st and 2nd side face, the 4th side face which countered this 3rd side face, and a top face, The source field and drain field which are prepared in said convex semi-conductor layer, and contain the electric contact section, respectively, It has the side-attachment-wall gate section prepared on the 1st side face at least in the condition of said convex semi-conductor layer of having insulated with this convex semi-conductor layer. The gate electrode which gives the electric field effect to the channel field between the gate electrode aforementioned source field which gives the electric field effect at least to the channel field between said source fields and said drain fields through the 1st side face of said convex semi-conductor layer, and said drain field is provided. For said electric contact section, a part of 1st side face of said convex semi-conductor layer, a part of 2nd side face and a top face, and the 3rd and 4th side face are the semiconductor device characterized by straddling either a part respectively.

[Claim 17] The convex semi-conductor layer formed on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. It is the semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and the gate length of said side-attachment-wall gate section being shorter than the gate length of said top-face gate section.

[Claim 18] The process which etches a semi-conductor substrate and forms a convex semi-conductor layer in this semi-conductor substrate, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, The process which forms a side-attachment-wall insulator layer on the side face of said gate electrode, and the side face of said convex semi-conductor layer, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode and said side-attachment-wall insulator layer for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 19] The process which forms the insulator layer which has puncturing on a semi-conductor substrate, and the process which forms a convex semi-conductor layer on the semi-conductor substrate exposed from said puncturing, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 20] Said convex semi-conductor layer is the manufacture approach of the semiconductor device according to claim 19 characterized by being formed by the epitaxial grown method.

[Claim 21] The process which forms a convex semi-conductor layer on a substrate, and the process which embeds the perimeter of said convex semi-conductor layer with an insulating material, The process which forms the slot for forming the side-attachment-wall gate section in said insulating material, The process which forms gate dielectric film on the side face of said convex semi-conductor layer exposed from said slot at least, The process which forms the gate electrode which has the side-attachment-wall gate section formed in said Mizouchi, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 22] Said side-attachment-wall gate section is a semiconductor device according to claim 1 characterized by having offset to a part of said source field and drain field.

[Claim 23] The semiconductor device according to claim 1 characterized by providing further a semi-conductor layer with high impurity concentration higher than said channel field prepared between said substrates and said source fields ranging over each between said substrates and said drain fields and between said substrates and said channel fields.

[Claim 24] It is the semiconductor device according to claim 1 characterized by providing the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and the 2nd gate dielectric film formed on the top face of said convex semi-conductor layer, and said 2nd gate dielectric film being thicker than said 1st gate dielectric film.

[Claim 25] Said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a forward tapered shape toward the top face of this convex semi-conductor layer from said substrate.

[Claim 26] The lower field of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a forward tapered shape toward the top face of this convex semi-conductor layer from said substrate.

[Claim 27] The configuration of the pars-basilaris-ossis-occipitalis corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a round configuration.

[Claim 28] The configuration of the up corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a round configuration.

[Claim 29] The include angle of the up corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by exceeding 90 degrees.

[Claim 30] The semiconductor device according to claim 1 characterized by providing further the insulating material prepared between said substrate and said convex semi-conductor layer, and the semiconductor region of the same conductivity type as said channel field being in each between the pars basilaris ossis occipitalis of said source field, and said insulating material, and between the pars basilaris ossis occipitalis of said drain field, and said insulating material.

[Claim 31] Said convex semi-conductor layer is a semiconductor device according to claim 30 characterized by being an amorphous silicon.

[Claim 32] For said electric contact section, said source field and a drain field are a semiconductor device according to claim 1 characterized by straddling respectively a part of side face of said convex semi-conductor layer, a part of other side faces which countered this side face, and the top face of said convex semi-conductor layer including the electric contact section, respectively.

[Claim 33] It is the semiconductor device according to claim 1 characterized by providing the 2nd gate dielectric film formed on the top face of the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and said convex semi-conductor layer, and said 2nd gate dielectric film being thinner than said 1st gate dielectric film.
[Claim 34] It is the semiconductor device according to claim 1 which possesses the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and the 2nd gate dielectric film formed on the top face of said convex semi-conductor layer, and is characterized by the configuration of the up corner of said 1st gate dielectric film being a round configuration.
[Claim 35] The distance between said source fields and said drain fields is a semiconductor device according to claim 1 characterized by becoming long toward the lower part from the upper part of said convex semi-conductor layer.
[Claim 36] The high impurity concentration of said source field and the high impurity concentration of said drain field are a semiconductor device according to claim 1 characterized by becoming low toward the lower part from the upper part of said convex semi-conductor layer.
[Claim 37] Said side-attachment-wall gate section is a semiconductor device according to claim 1 characterized by being formed in the bottom of said source field and said drain field along two side faces in which it faces mutually [said convex semi-conductor layer].
[Claim 38] The width of face of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being smaller than 0.2 micrometers.
[Claim 39] The width of face of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being smaller than the depth of said source field, and the depth of said drain field.
[Claim 40] At least one of said source field and said the drain fields is a semiconductor device according to claim 1 characterized by including two kinds of diffusion layers of a high concentration diffusion layer with deep high impurity concentration, and a low concentration diffusion layer with high impurity concentration thinner than said high concentration diffusion layer at least.
[Claim 41] Said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by connecting with said substrate electrically.
[Claim 42] Said substrate is a semiconductor device according to claim 1 characterized by being conductivity.
[Claim 43] It is the semiconductor device according to claim 1 which possesses further the gate dielectric film formed between each of two side faces in which said side-attachment-wall gate section is faced mutually [said convex semi-conductor layer], and is characterized by said gate dielectric film consisting of an oxide of Ta, Sr, aluminum, Si, Zr, Hf, La, and Ti which contains any one at least.

[Translation done.]

* NOTICES *

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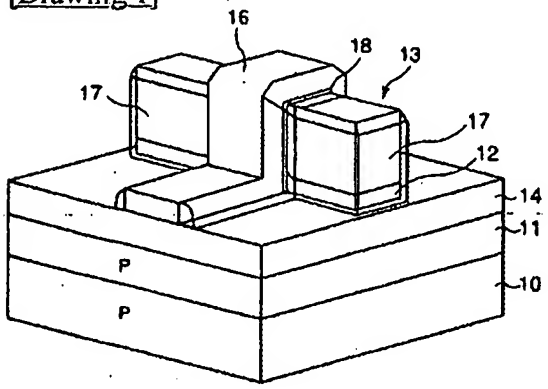
DRAWINGS

[Drawing 1]



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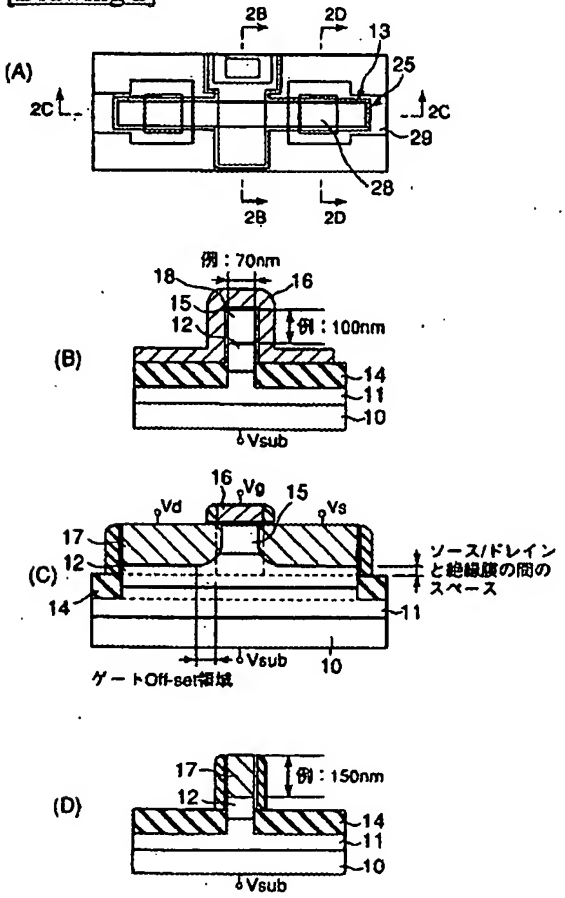

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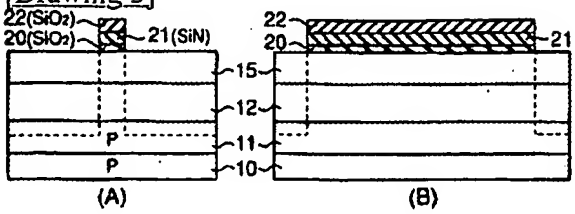

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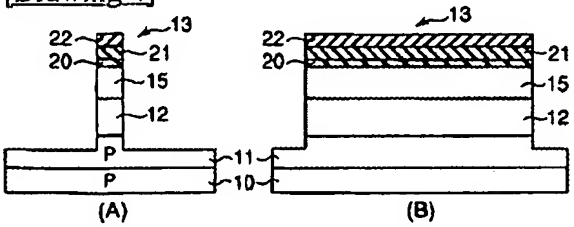

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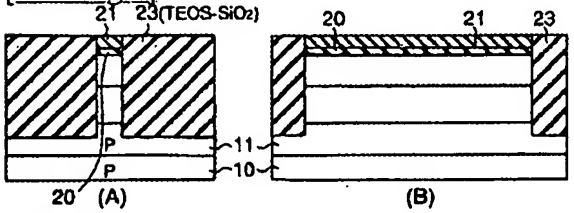

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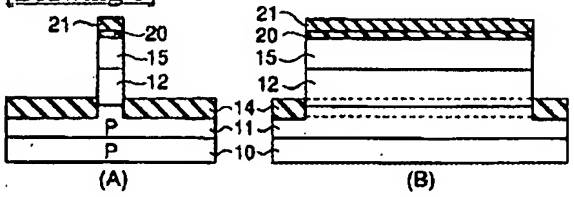

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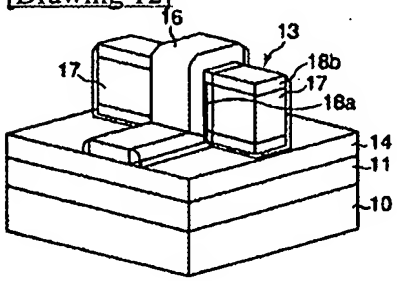

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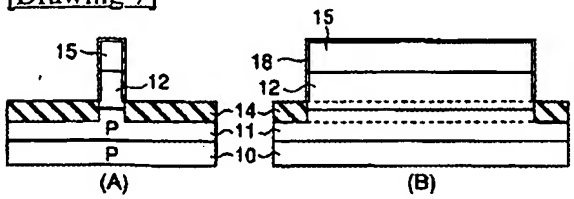

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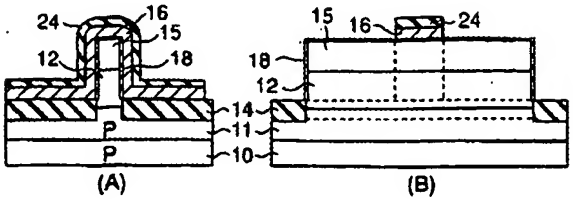

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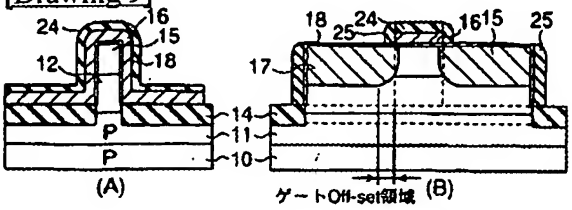

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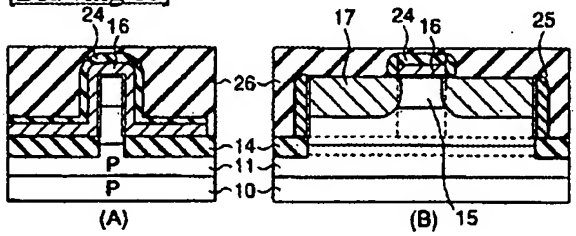

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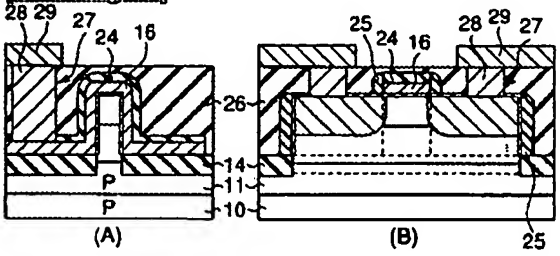

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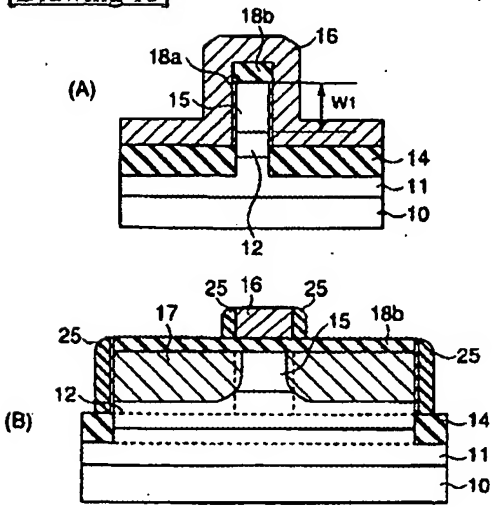

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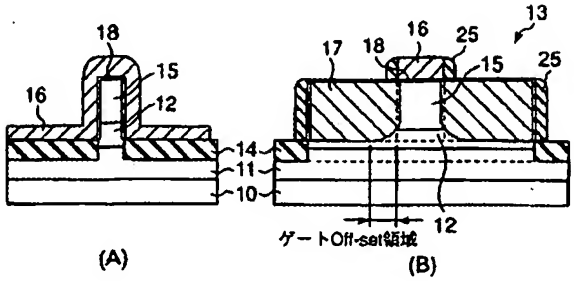

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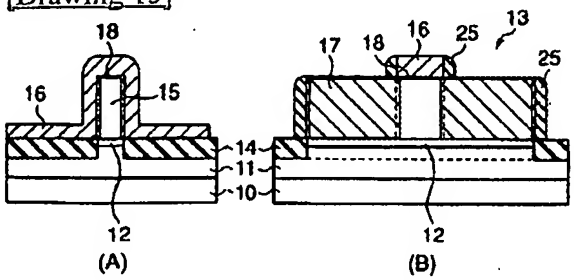

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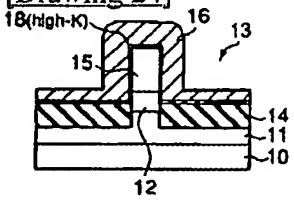
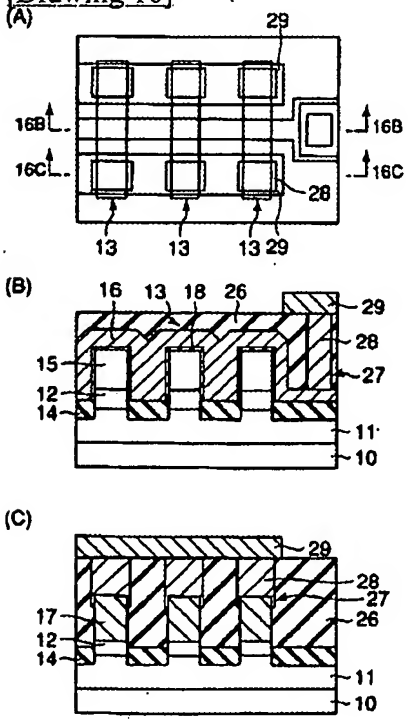


[Drawing 16]



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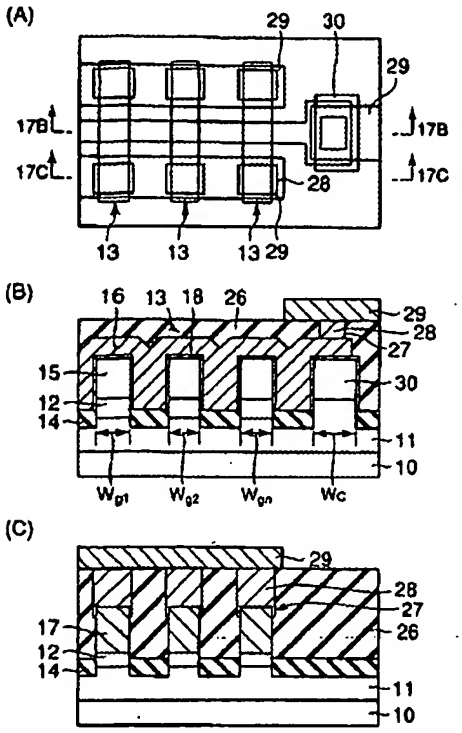

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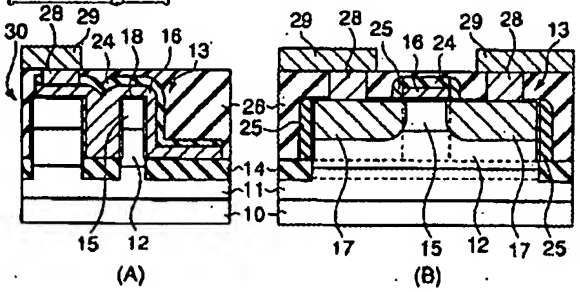
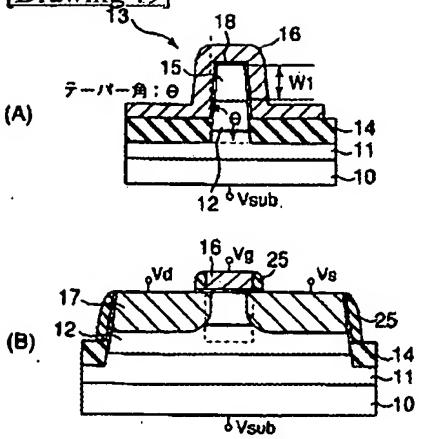


[Drawing 19]



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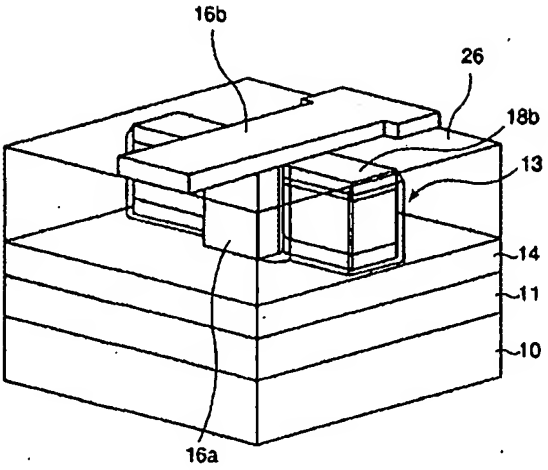

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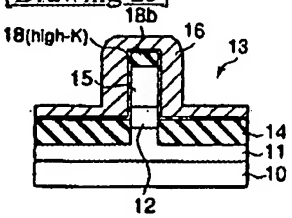

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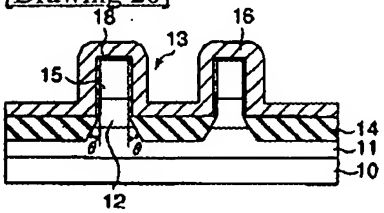

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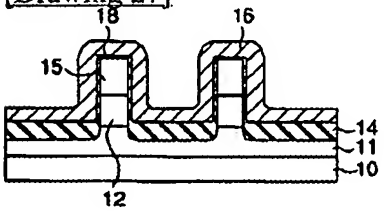

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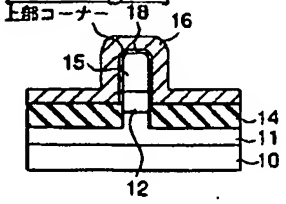

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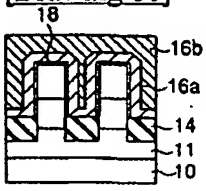

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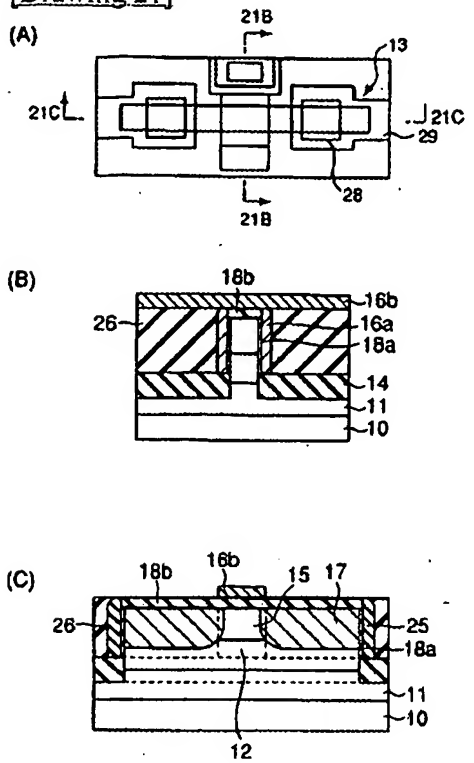

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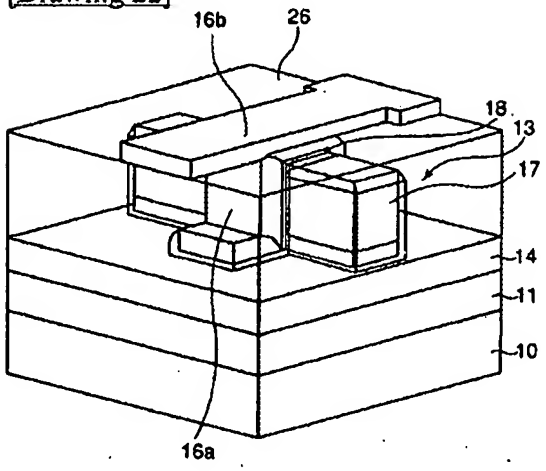
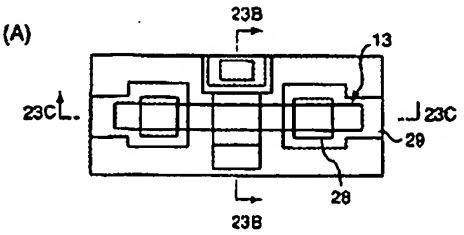
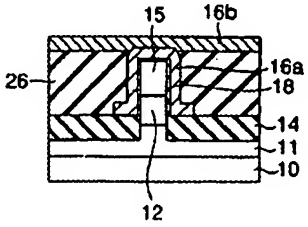


[Drawing 23]

(A)



(B)



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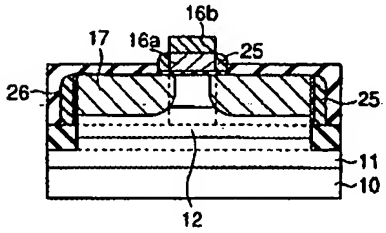

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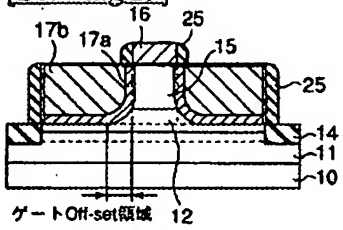

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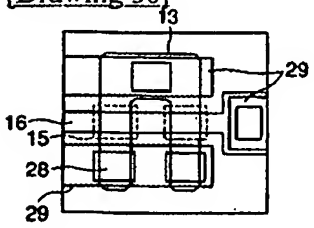

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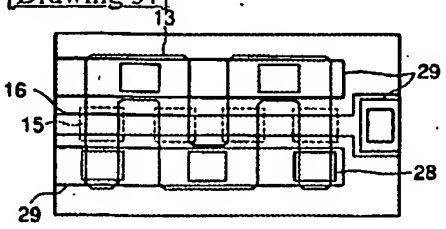

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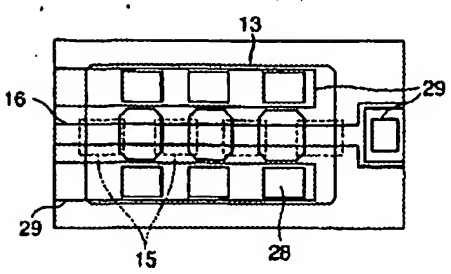

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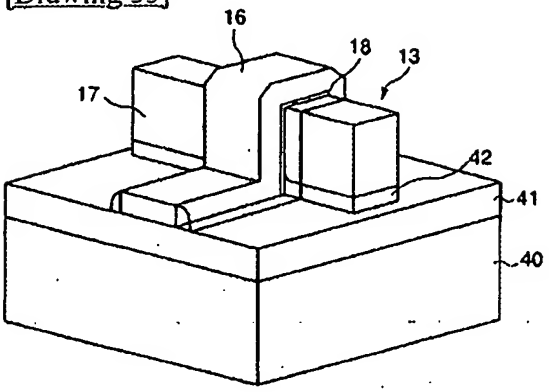

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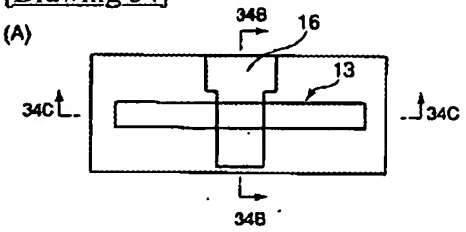

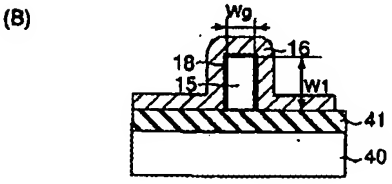

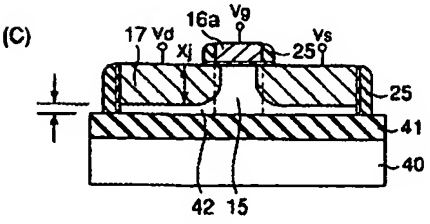

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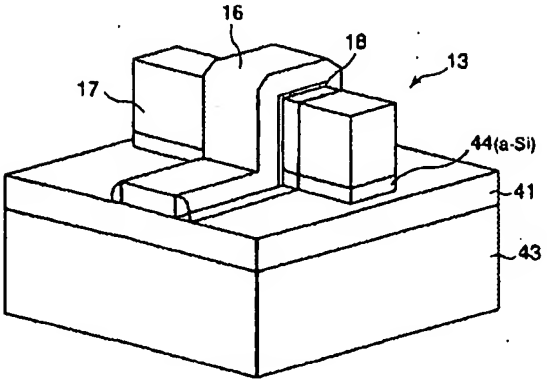

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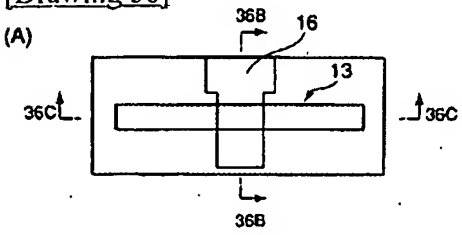
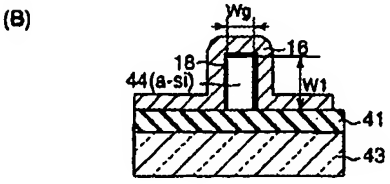
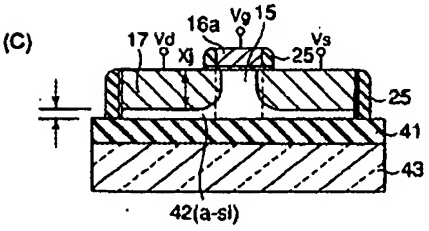
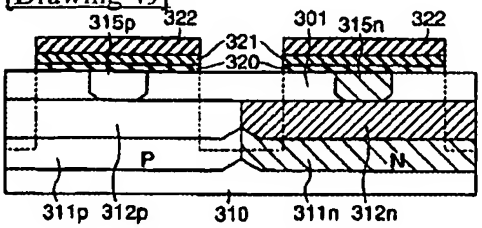






[Drawing 49]



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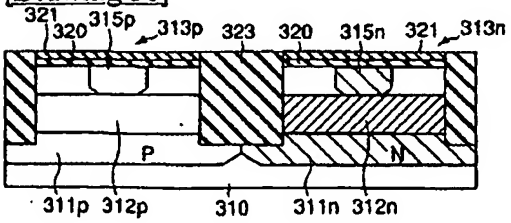

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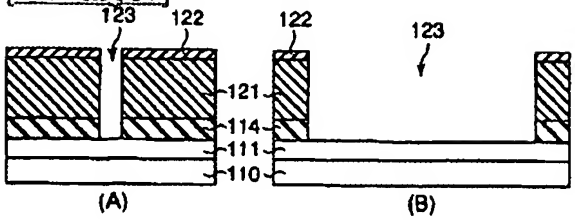

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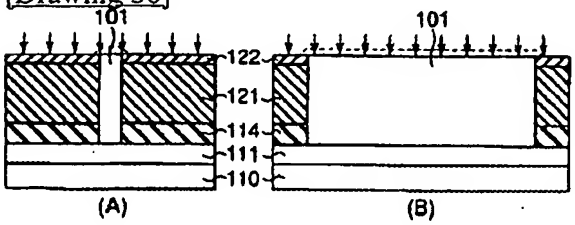

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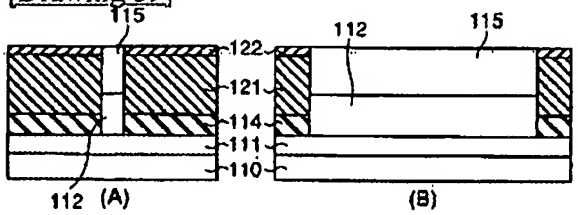

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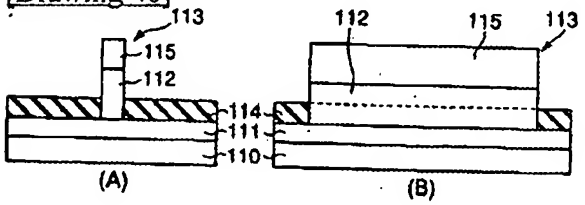

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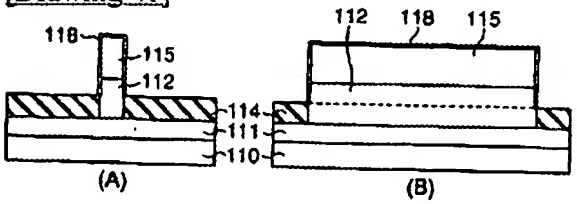

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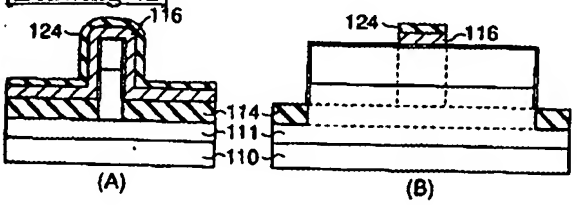

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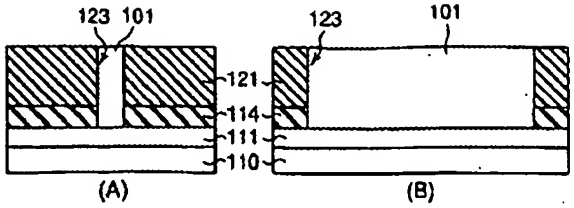

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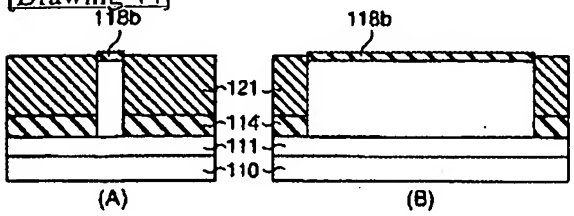

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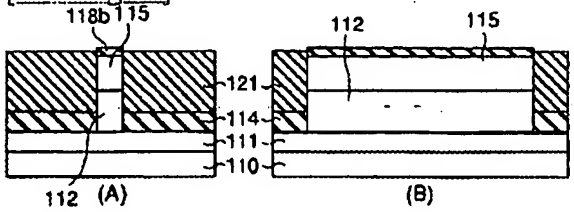

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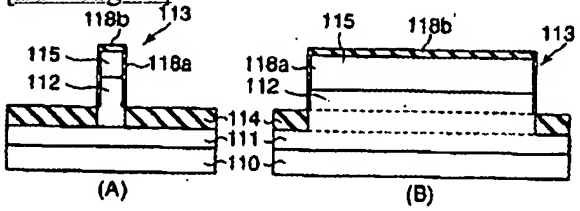

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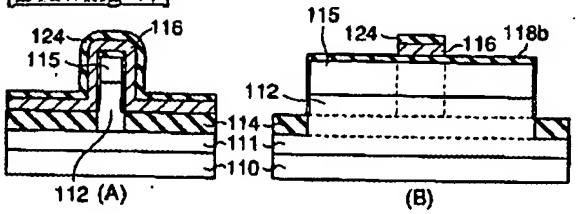

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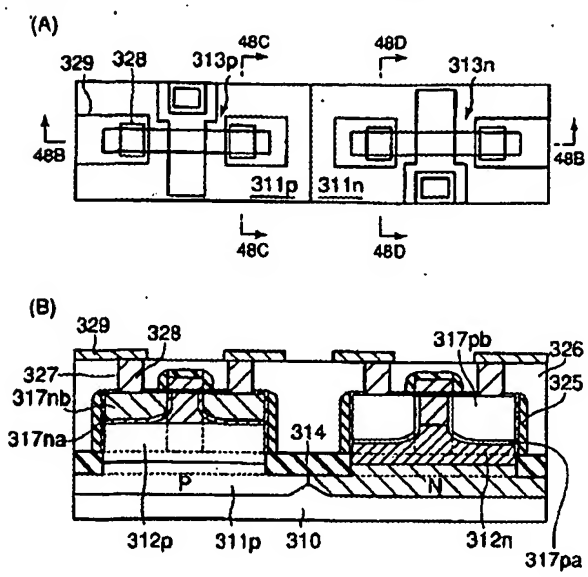

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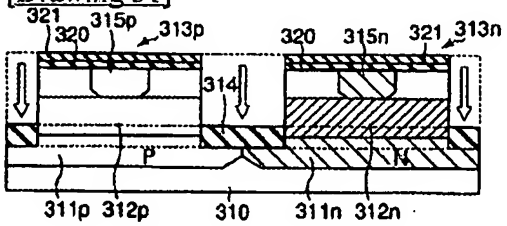

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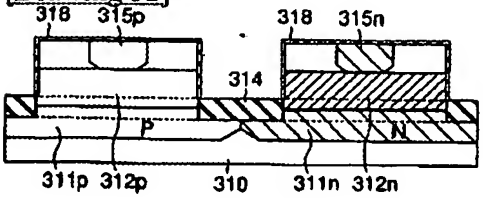

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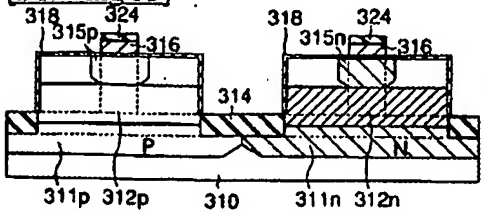

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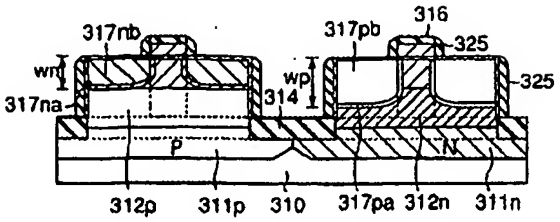

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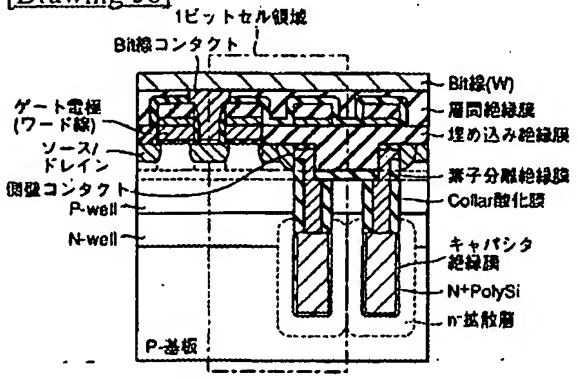
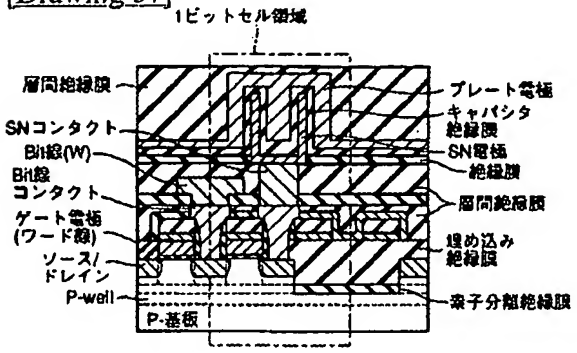


[Drawing 57]



[Drawing 55]

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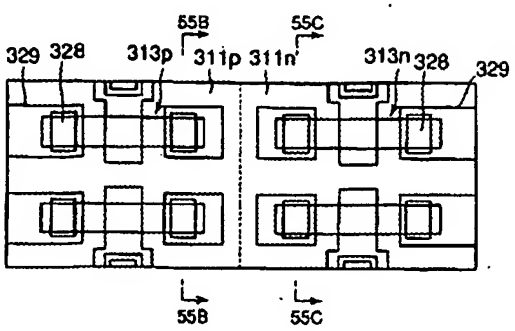
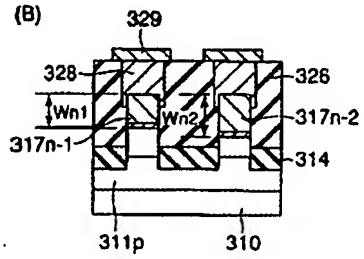


(B)



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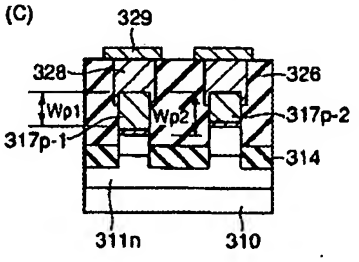

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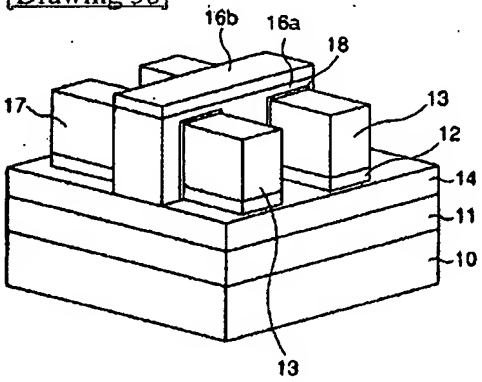

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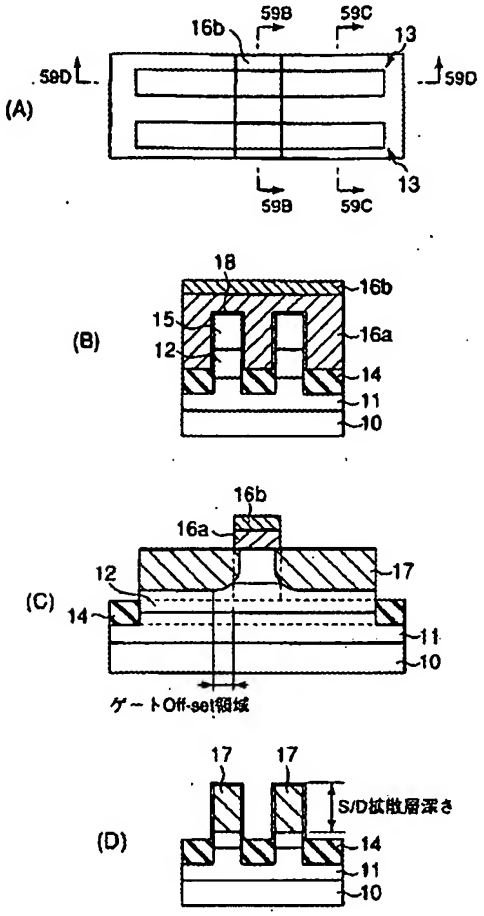

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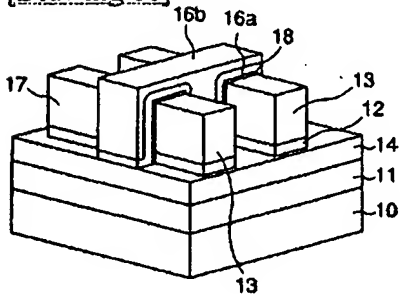

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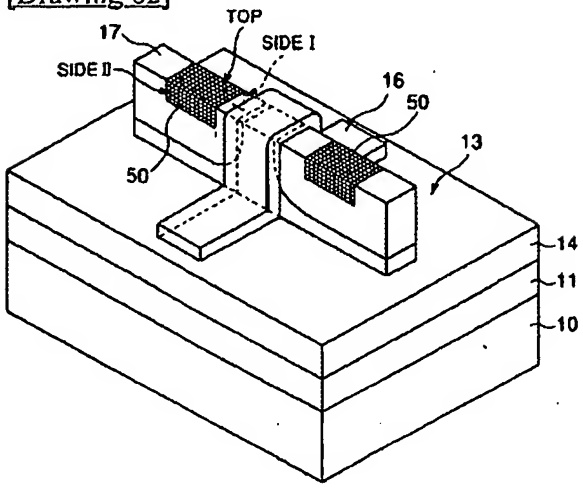
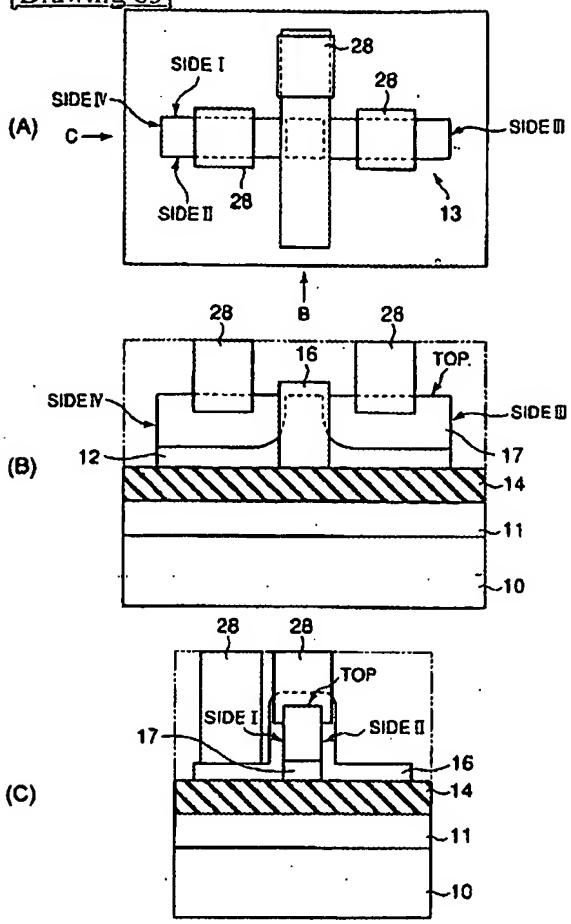


[Drawing 63]



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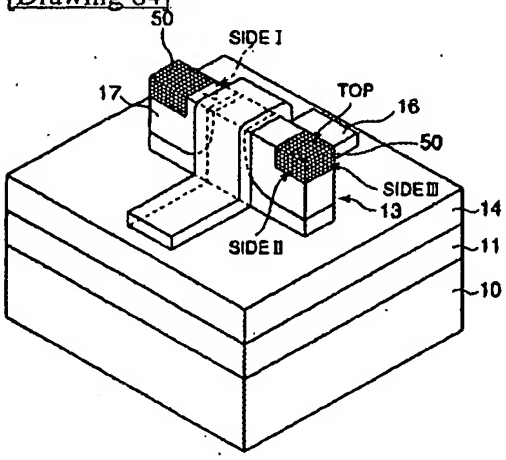

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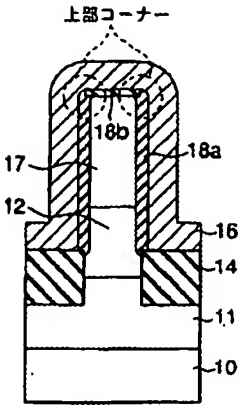

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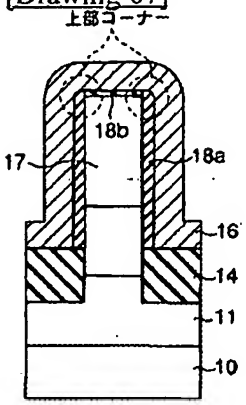
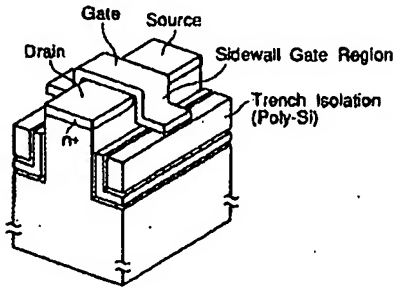
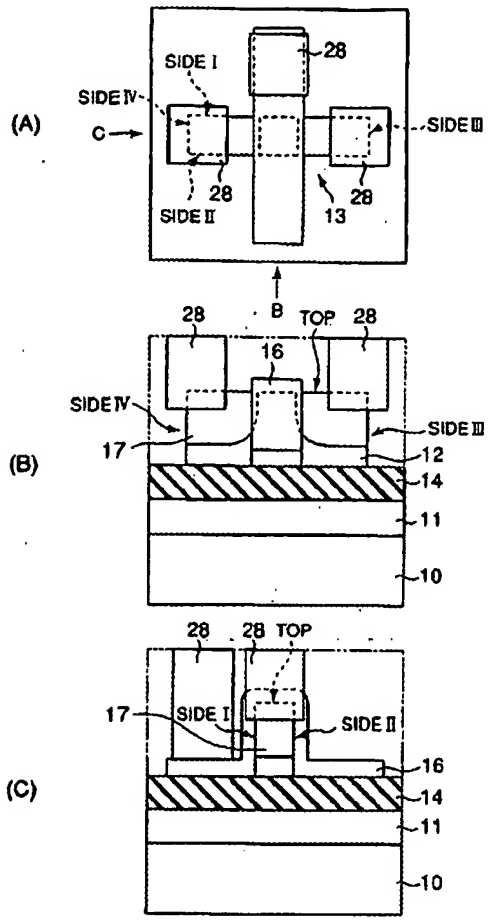


[Drawing 79]

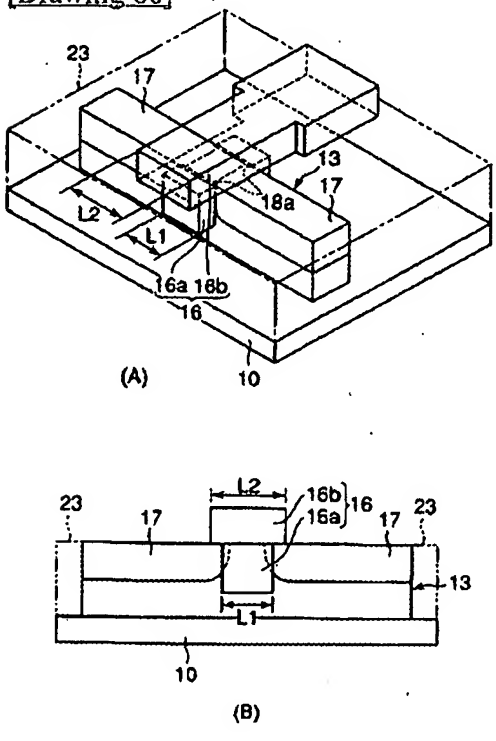
Trench Isolated (TIS) Transistor (1987 IEDM)



[Drawing 65]

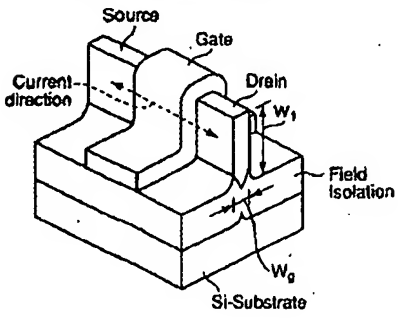


[Drawing 68]



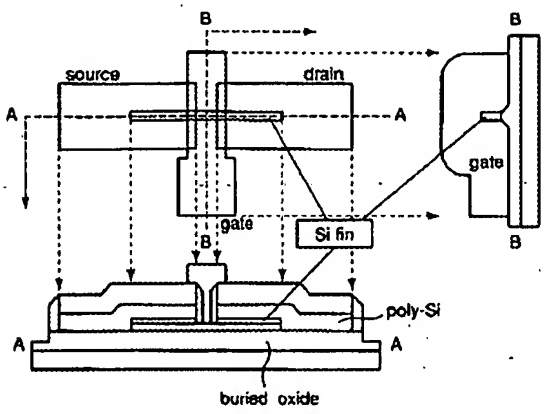
[Drawing 80]

DELTA構造 (1989 IEDM)

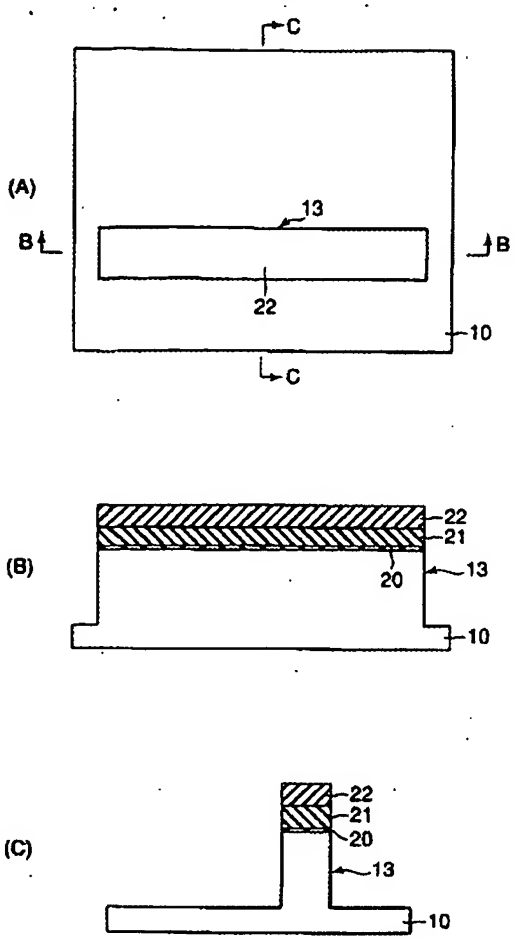


[Drawing 81]

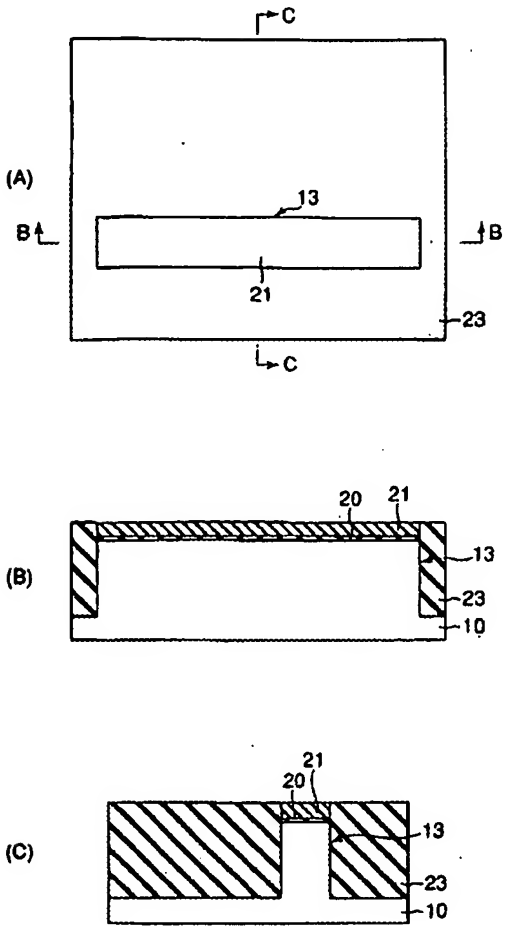
Folded-channel MOSFFT (1998 IEDM)



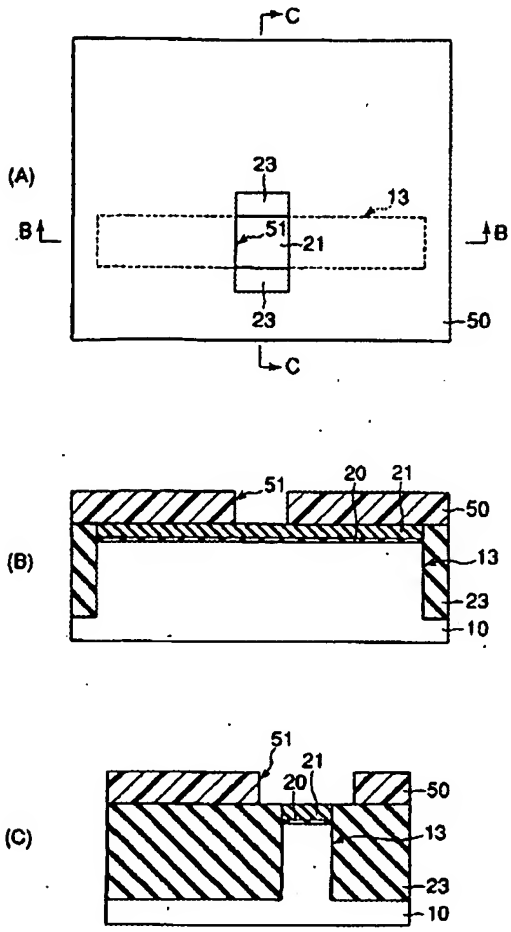
[Drawing 69]



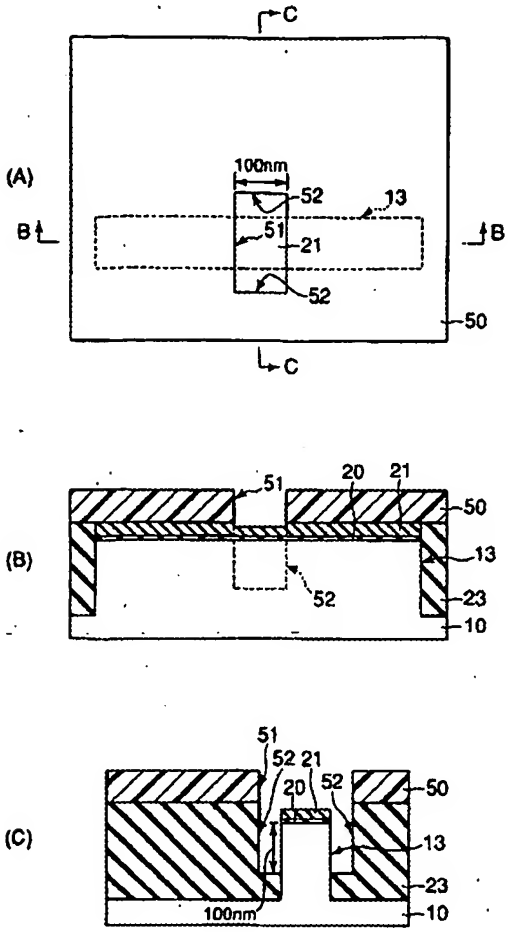
[Drawing 70]



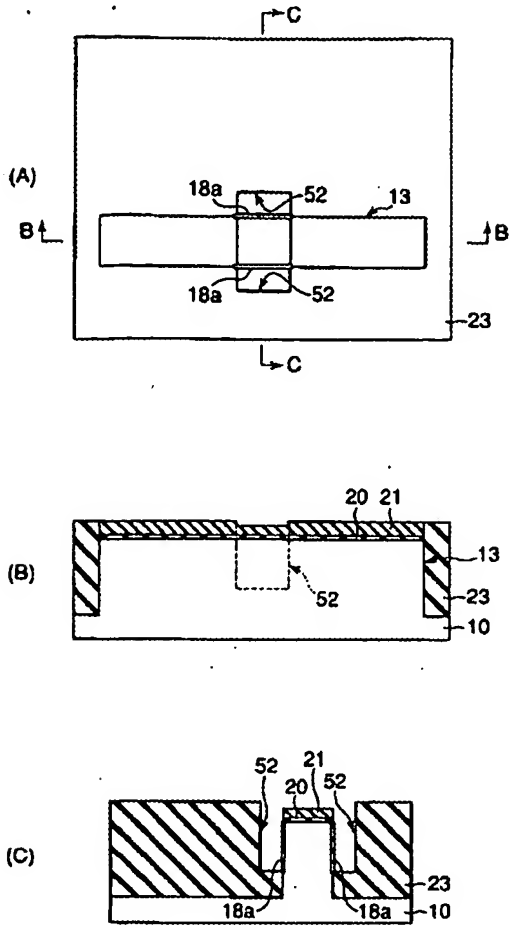
[Drawing 71]



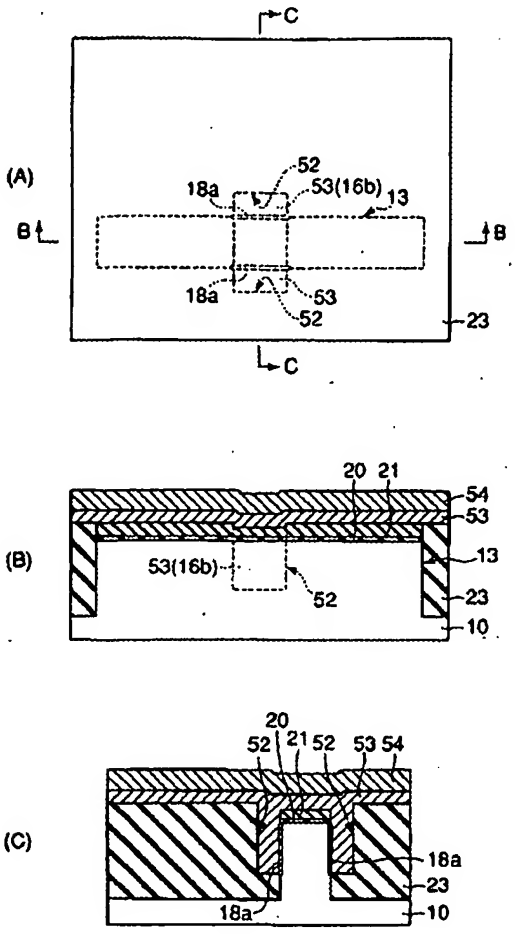
[Drawing 72]


C
(A)
100nm
52
13
B
51
21
B
52
50
C
(B)
51
20
21
50
13
52
23
10
(C)
51
52
21
20
52
50
13
23
100nm
10

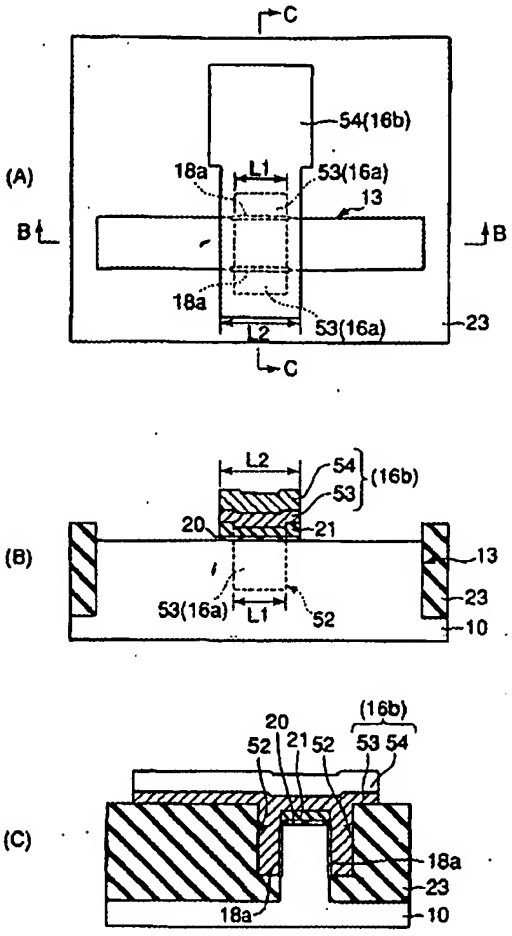
[Drawing 73]


C
(A)
18a
52
13
B
B
18a
52
23
C
20 21
(B)
13
52
23
10
52
21
20
52
(C)
23
18a
18a
10

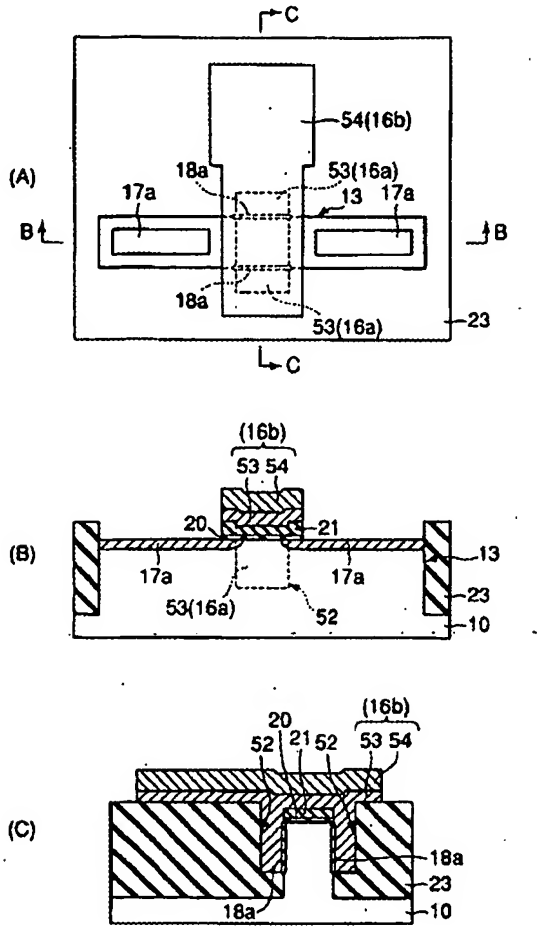
[Drawing 74]


(A)
C
B
B
C
52
18a
53(16b)
13
18a
53
52
23
(B)
20
21
54
53
53(16b)
13
52
23
10
(C)
20
52
21
52
53
54
18a
23
18a
10

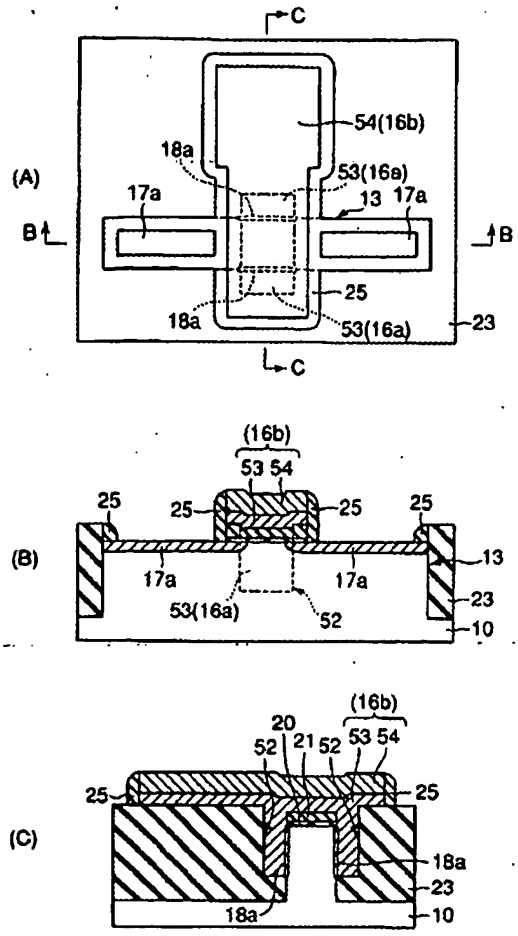
[Drawing 75]


(A)
C
54(16b)
18a
L1
53(16a)
13
B
B
18a
53(16a)
L2
23
C
(B)
L2
54
53
(16b)
20
21
13
23
53(16a)
L1
52
10
(C)
20
52
21
52
(16b)
53
54
18a
23
18a
10

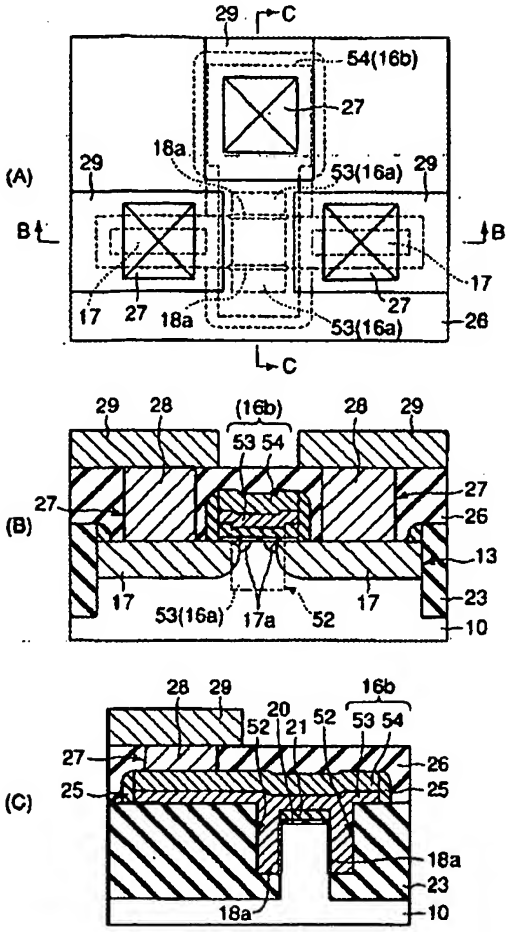
[Drawing 76]


C
54(16b)
(A)
18a
53(16a)
17a
13
17a
B
B
18a
53(16a)
23
C
(16b)
53 54
20
21
(B)
13
17a
17a
23
53(16a)
52
10
20
(16b)
52
21
52
53 54
(C)
18a
23
18a
10

[Drawing 77]


C
54(16b)
18a
53(16a)
(A)
17a
13
17a
B
B
25
18a
53(16a)
23
C
(16b)
53 54
25
25
25
25
(B)
13
17a
17a
23
53(16a)
52
10
(16b)
20
52
21
52
53 54
25
25
(C)
18a
23
18a
10

[Drawing 78]



[Translation done.]